

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

~~Claims 1-14 have been canceled~~ Claims 1-14 (Canceled).

Claims 15-34 have been canceled.

Claim 35 (New): A bit stream processor, comprising:

a memory having one or more inputs for receiving respective input bit streams, said input bit streams of said one or more inputs defining a sequence of input combinations to said memory;

an opcode input of said memory for inputting a selected opcode, which said selected
5 opcode is composed of all possible results of a logical function operating on an input combination;

an output of said memory for outputting an output bit stream;

wherein each input combination addresses a bit of the selected opcode stored in the memory to generate an output bit.

Claim 36 (New): The bit stream processor of Claim 35, wherein said memory is a bit-addressable memory where each said input combination of said sequence of input combinations is mapped to a unique bit location in said memory.

Claim 37 (New): The bit stream processor of Claim 35, wherein said memory comprises binary memory devices which can be individually and selectively read.

Claim 38 (New): The bit stream processor of Claim 35, wherein said logical function is a function of one or more Boolean operations.

Claim 39 (New): The bit stream processor of Claim 35, wherein each of said one or more inputs accommodates a serial bit stream.

AMENDMENT AND RESPONSE

S/N 09/389,567

Atty. Dkt. No. NEXQ-24,727

Claim 40 (New): The bit stream processor of Claim 35, wherein said opcode is composed of the results of a logical function defined by a predetermined set of Boolean operations.

Claim 41 (New): A method for bit stream processing, comprising the steps of:

providing a memory having one or more inputs for receiving respective input bit streams, the input bit streams of the one or more inputs defining a sequence of input combinations to the memory;

inputting a selected opcode at an opcode input of the memory, which said selected
5 opcode is composed of all possible results of a logical function operating on an input combination;

storing said selected opcode in said memory such that each bit of the stored selected opcode is equal to the result of the logical function operating on an input combination;

outputting an output bit stream at an output of the memory, wherein said output bit stream is composed of the sequence of bits of the selected opcode addressed by the input bit streams..

Claim 42 (New): The method of claim 41, wherein the memory in the step of providing is a bit-addressable memory where each input combination of the sequence of input combinations is mapped to a unique bit location in the memory.

Claim 43 (New): The method of claim 41, wherein the memory in the step of providing comprises binary memory devices which can be individually and selectively read.

Claim 44 (New): The method of claim 41, wherein the sequence of input combinations form a sequence of memory addresses.

Claim 45 (New): The method of claim 41, wherein the logical function is a function of one or more Boolean operations.

Claim 46 (New): The method of Claim 41, wherein each of the one or more inputs accommodates a single serial bit stream.

AMENDMENT AND RESPONSE
S/N 09/389,567
Atty. Dkt. No. NEXQ-24,727